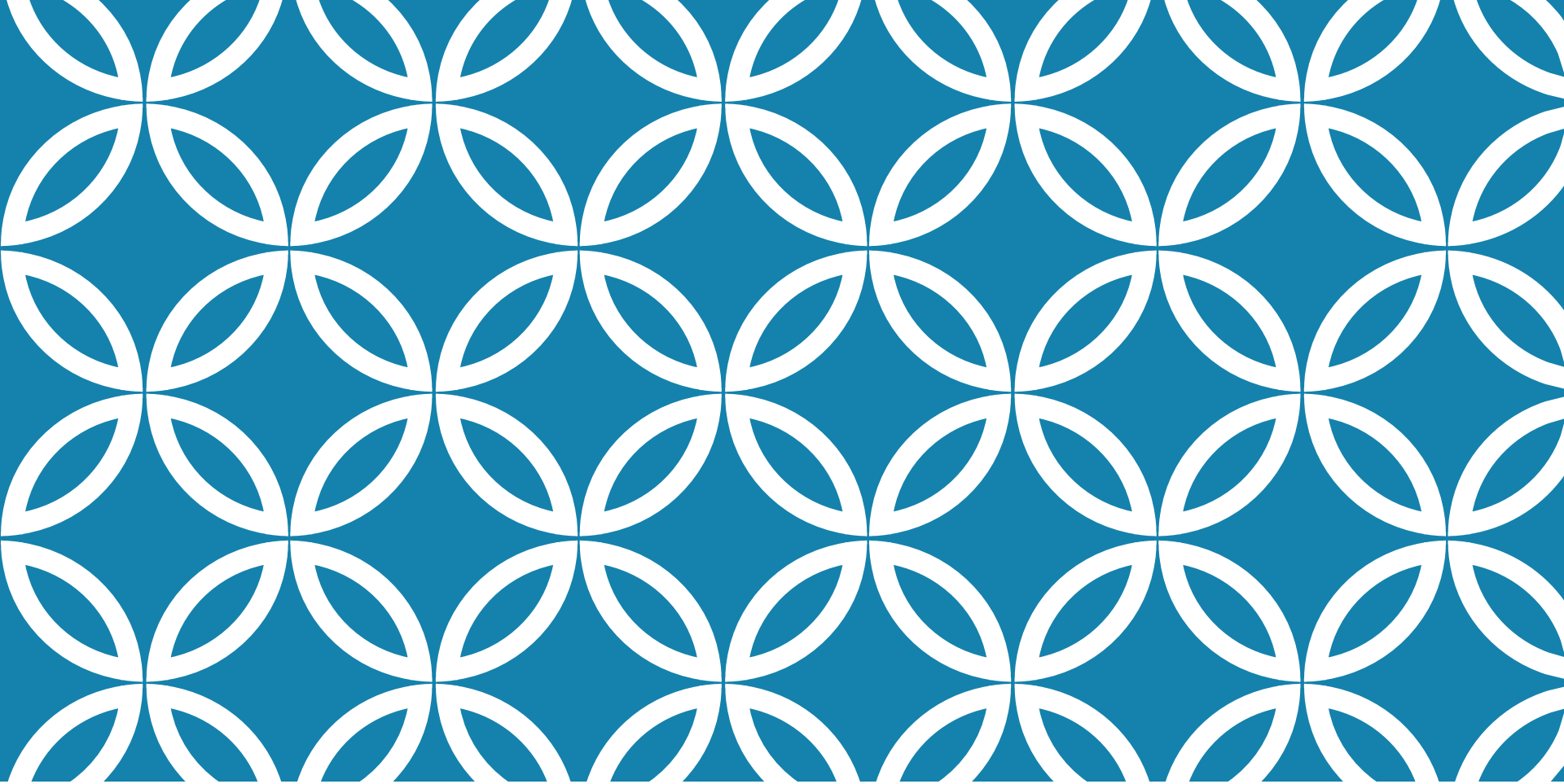


R&D ON ELECTRONIC DEVICES AND CIRCUITS FOR THE HL-LHC

Alberto Stabile
UNIMI and INFN - Milano

MAIN AIM AT HIGH LUMINOSITY-LHC

Common goal: identification of particle tracks in vertex detector

Pixel detector

- Resolution <10 μm
- 10^6 particles mm^{-2} s^{-1}
- Dose 1 Grad

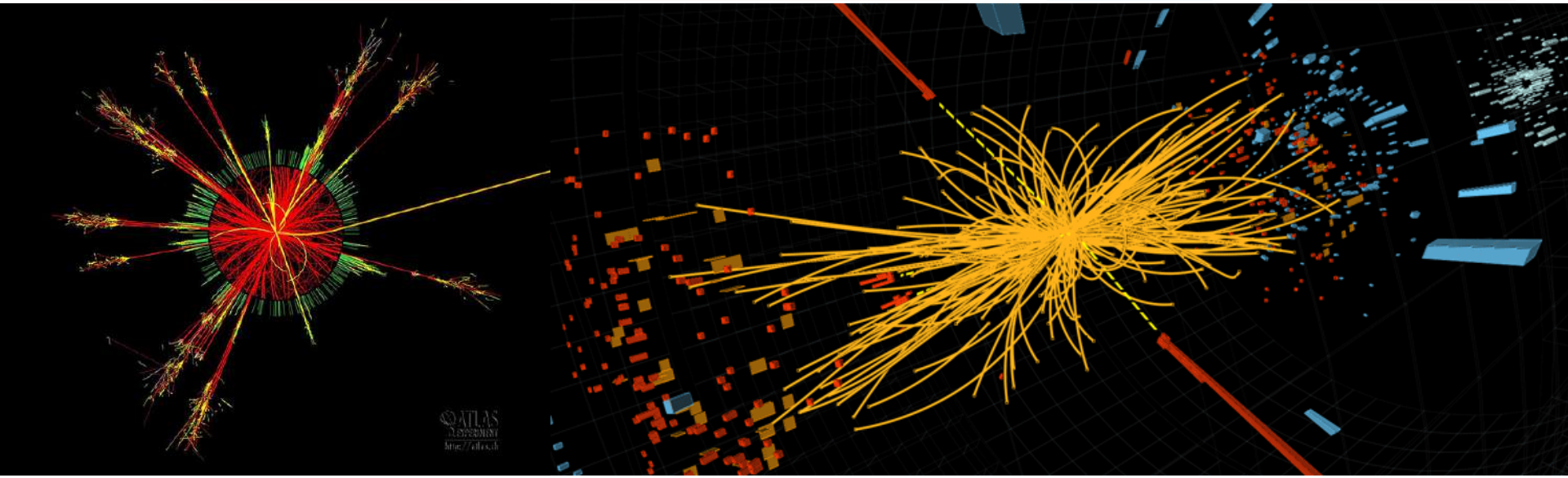
Huge amount of produced data

- **Limited** amout of events can be transferred

Data reduction must be performed

Trigger system

- Particle track recognition in **real time**
- **CPUs** of HLT not suitable for this task



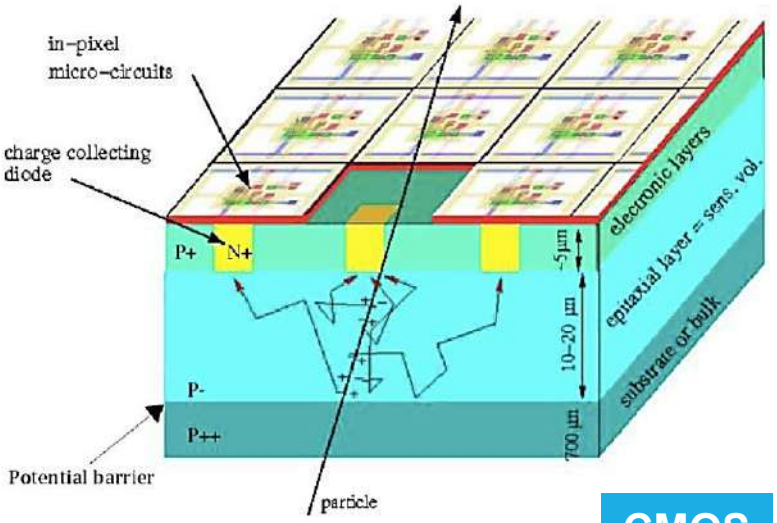
CMOS PIXEL DETECTOR

Alberto Stabile

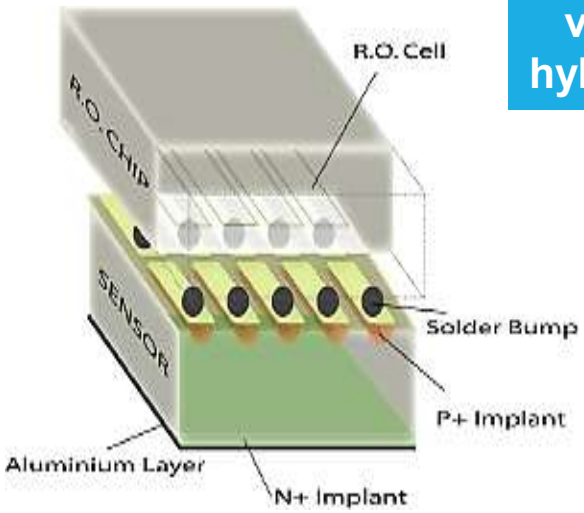
CMOS PIXEL DETECTORS

CMOS detector:

- integrate 2 devices that normally in hybrid detector are separated:
  - detector + front-end electronics
  - readout electronics
- commercial technology:
  - large volume
  - low cost productions
- low resistivity substrate (1-10 Ω·cm):
  - very small depletion region
- charge collection by diffusion
  - charge carriers diffuse in the substrate
  - until either recombine or are collected by an electrode
  - long collection time / partial charge collection



CMOS vs. hybrid



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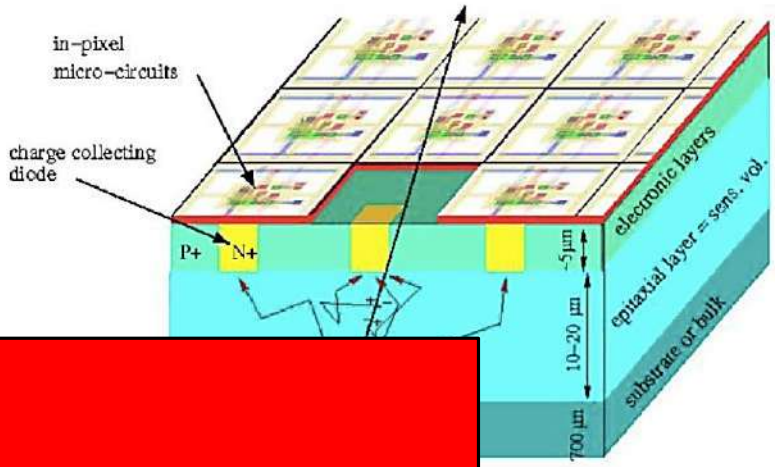
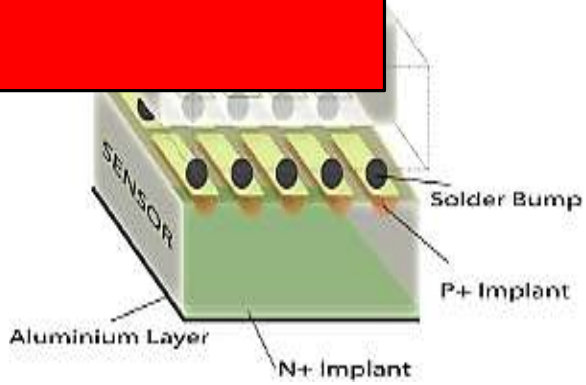


not suitable for high rate application ☹
not enough radiation hard ☹

CMOS vs. hybrid

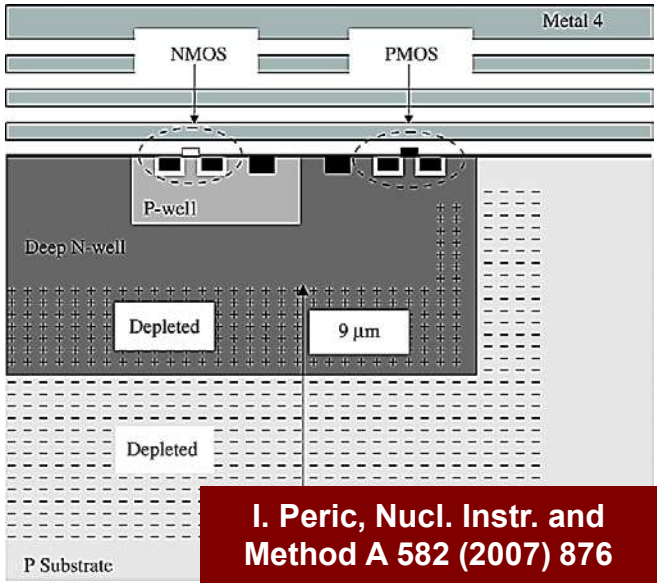


SOLUTION:
DEPLETED CMOS DETECTORS

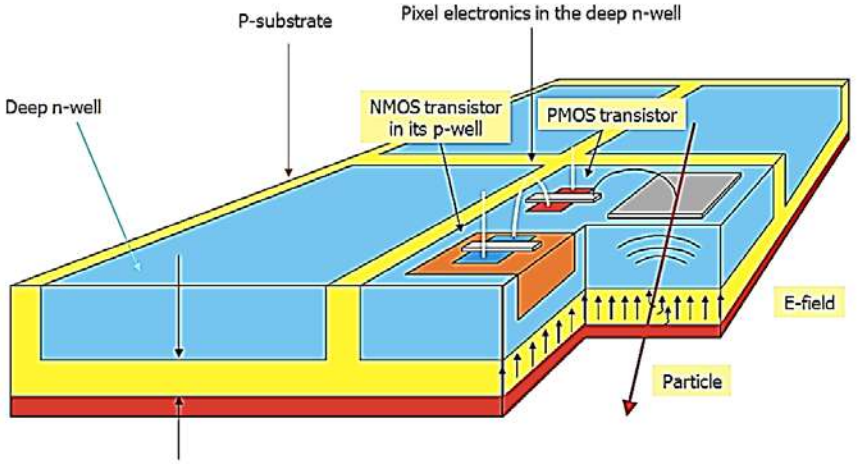
Depletion depth: $d = \sqrt{\epsilon_{si}\epsilon_0\mu_{carrier}\rho(V + V_{BI})}$

Enabling technologies:

- **High Voltage** processes
  - Availability of processes with high voltage capability, driven by automotive and power management applications
- **High Resistivity** substrates
  - Foundries accepting/qualifying wafers or epitaxial substrates with mid-high resistivity
- **130-180 nm feature size**
  - deep submicron technologies needed for the design of radiation hard electronics
  - multiple-well process to decouple front-end electronics from the sensitive region



I. Peric, Nucl. Instr. and Method A 582 (2007) 876



MONOLITHIC DETECTOR STATUS

Depleted-CMOS sensors are undergoing an active R&D phase

Many progresses have been achieved on the CMOS sensors

- Good understanding of the depletion zone and charge collection
- **Efficiency is >99%** even after irradiation at **fluences >10^{15} n_{eq}/cm^2**
- Encouraging results **for small fill factor design**
  - Low input capacitance and low power

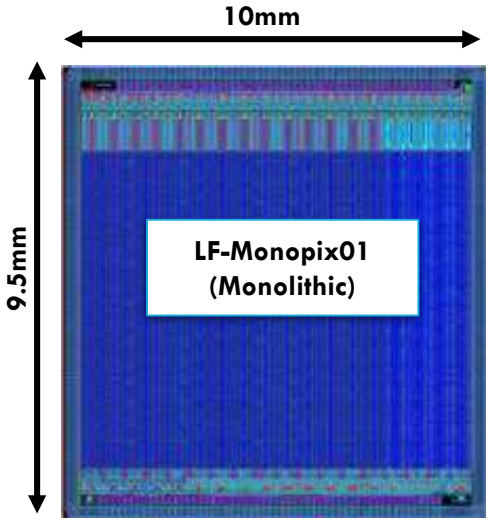
The major next R&D step is the integration of the sensors with a **high rate readout architecture**

- Development of **fast-thin-radiation hard CMOS sensors** will provide an interesting opportunity for future tracking detectors

MONOLITHIC PROTOTYPES

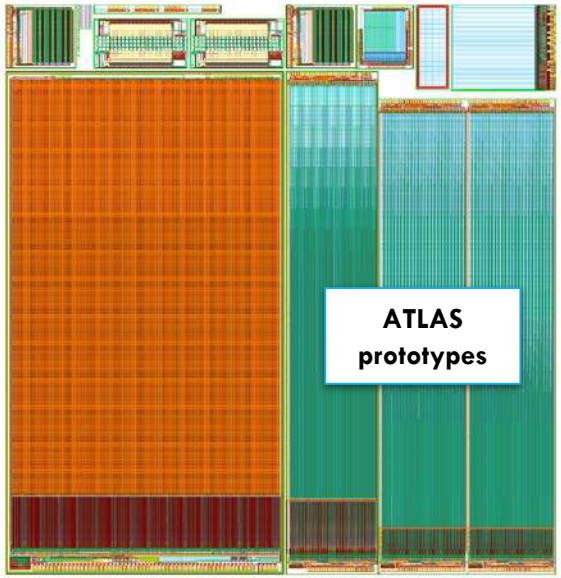
LFoundry

- Subm. in **Aug. 2016**
- **Monopix01** and **Coolpix1**
- "Demonstrator size"
- 50 x 250 μm^2 pixels
- Fast standalone R/O
- Column drain approach



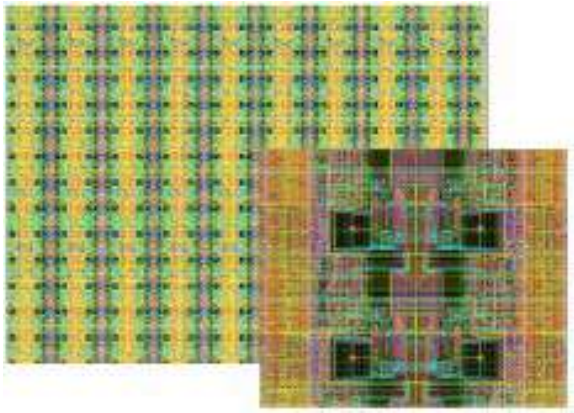
AMS H180

- Subm. in **Jan. 2017**
- **Mu3E** + **ATLAS** (monolithic)
- Additional production step – isolated PMOS
- 80 and 200 Ωcm wafers
- Reticle size about 21mm x 23mm



TowerJazz

- Subm. in **May 2017**
- Two large scale demonstrators **MALTA** and Monopix:
  - Focus on small fill-factor pixels
  - Asynchronous matrix readout (no clock distribution over the matrix)
  - Column Drain Read-Out (based on Monopix)



FAST TRACKING WITH **ASSOCIATIVE MEMORY CHIP**

Alberto Stabile

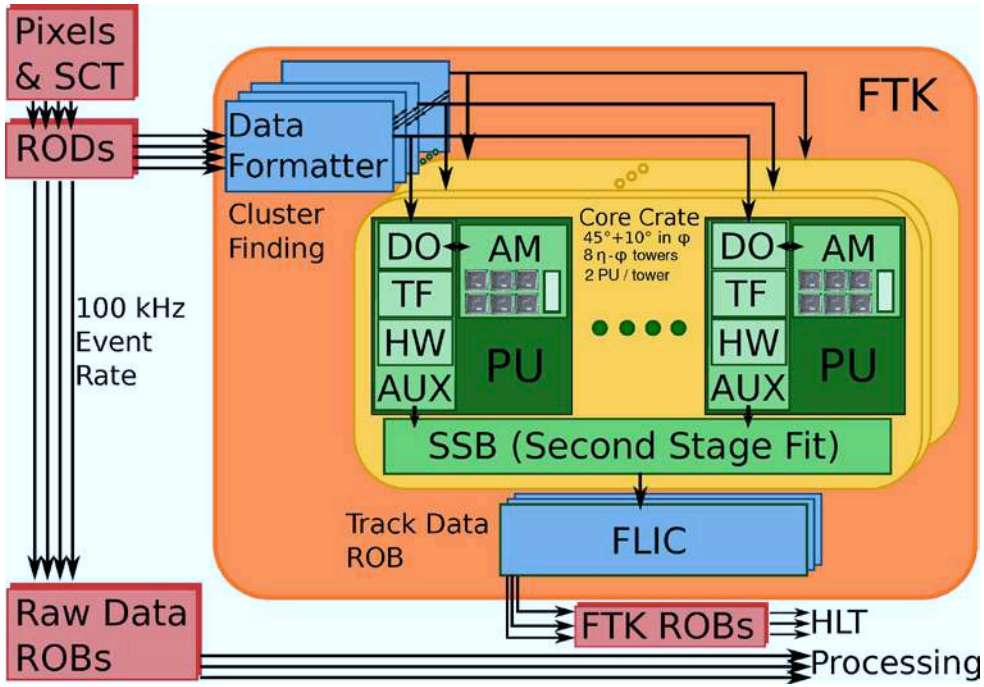
STATE-OF-THE-ART: THE FTK SYSTEM

The whole FastTraKer (FTK) system stores **one billion (10^9) patterns**

- **8 Mpatterns** per board (128 boards)
- **128 kpatterns** per chip (64 AM chips / board)
- A pattern is composed by 18 bits × 8 words

Major concerns:

- high pattern density
  - **large silicon area**
- I/O signal congestion at board level (**solution: 2 Gbit/s serial links**)
- Maximum power limited by cooling (because we are fitting 8192 AMchips in 8 VME crates): **250 W per AM board**

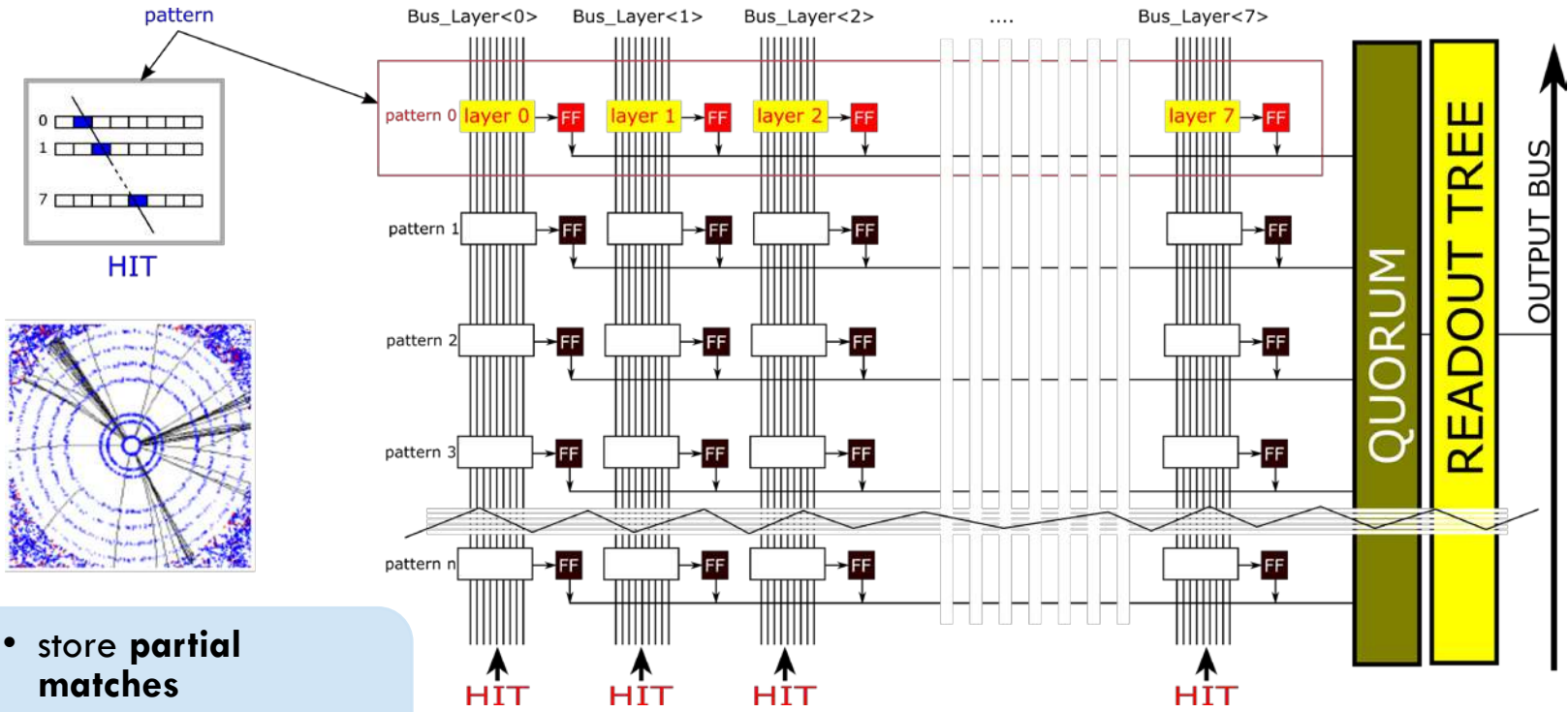


[1]A. Andreani et al., \The AMchip04 and the processing unit prototype for the FastTracker," *IOP J. Instr. 7* (2012) C08007

THE AM CHIP ARCHITECTURE

For each bus and for each pattern there is a small **CAM cell array (layer x)**

- It compares its own content with all data received. If it matches a **memory is set (FF)**
- The partial matches are analyzed by **Quorum logic** the and compared to the desired threshold
- A **readout encoder (Fischer Tree)** reads the matched patterns in order



The AM and commercially available CAMs differs substantially

The AM provides the unique capability:

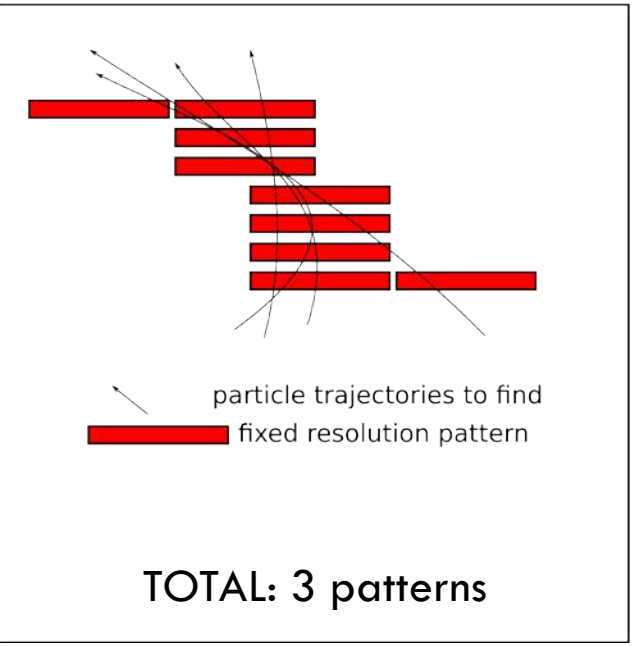
- store **partial matches**
- find correlations at **different times**

VARIABLE RESOLUTION

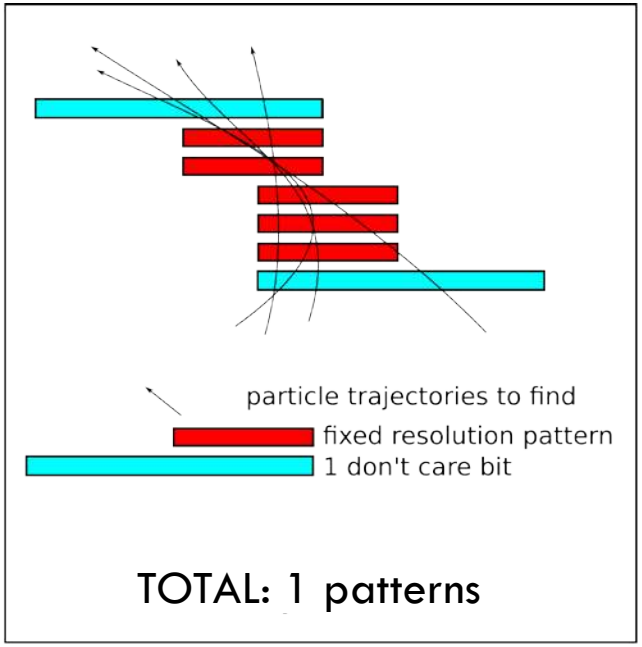
Smart approach: consists in performing pattern matching at **reduced and variable resolution first,** and then to **refine** matching resolution using a FPGA.

- A **"don't care" bit** is used to increase the pattern recognition efficiency at different resolutions.

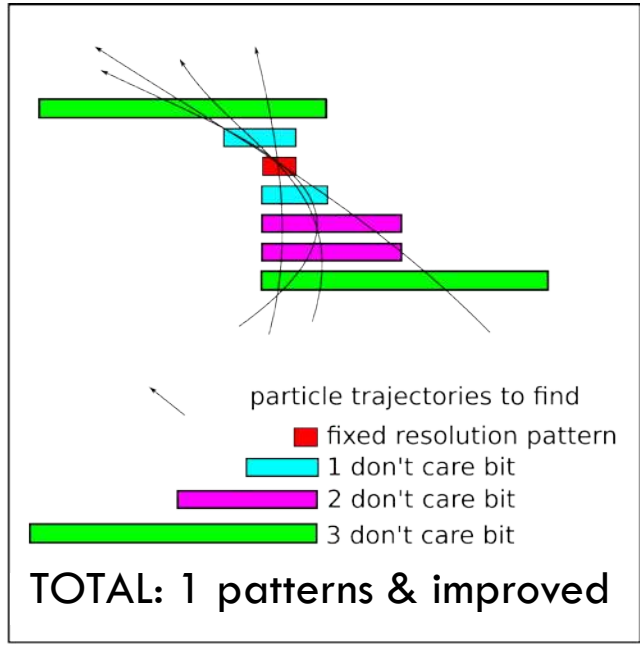
At high efficiency: number of fakes, required patterns, and power consumption decrease.



TOTAL: 3 patterns



TOTAL: 1 patterns



TOTAL: 1 patterns & improved

HL-LHC REQUIREMENTS

Big challenges from phase-II conditions

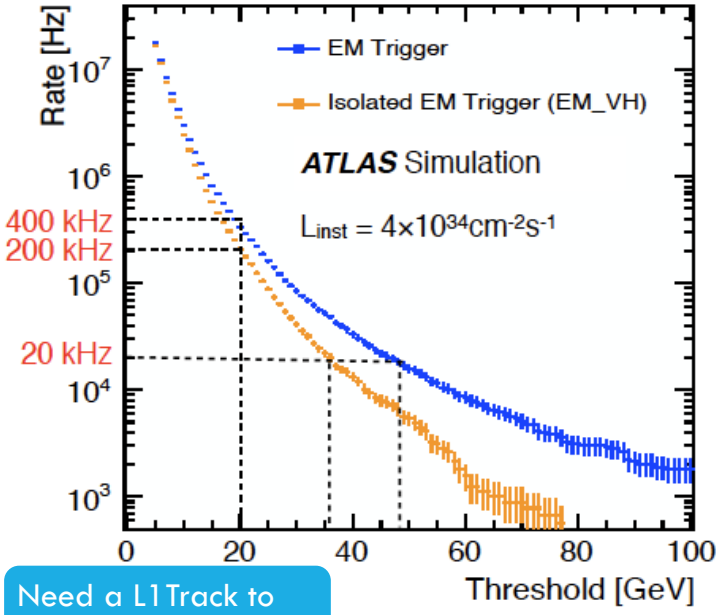
- Pileup 140 (max 200)

Track Triggers are a crucial piece of the phase-II upgrade plan

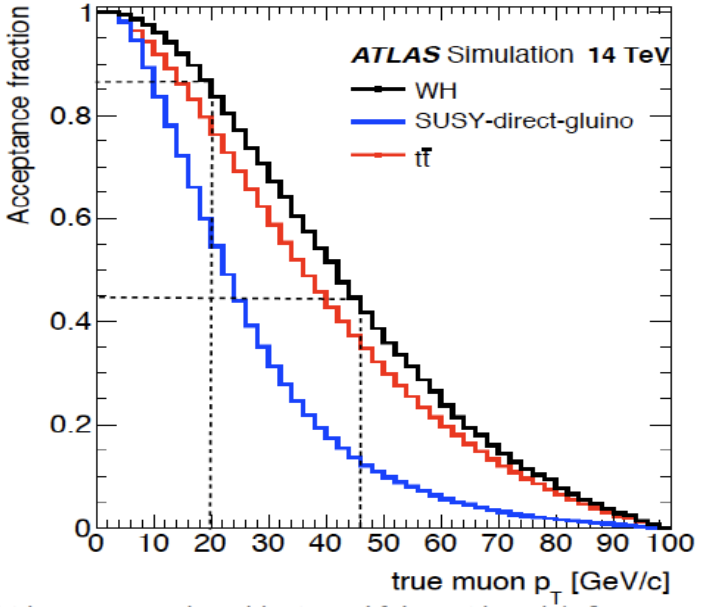
- **ATLAS:** L1Track and L2 upgrade
- **CMS:** L1Track Trigger is the baseline

Goal: evolve the system design to phase-II environment

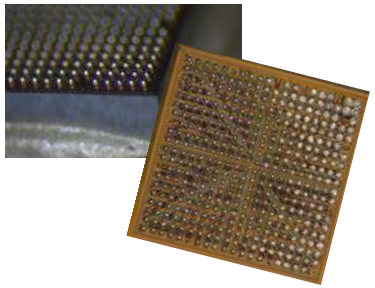
- **AM chip R&D**
- Fully exploit **ATCA** potentialities



Need a L1Track to save EM pt>20 GeV



AMCHIP TREND



Since 2010:

- **AM chip v. 4** designed and characterized 2012 – area: 14 mm² – cost: 50 k€ – 8 kpattens

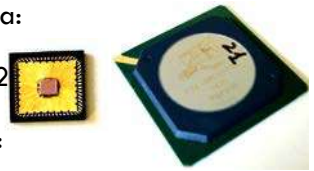
2015-2017
IMPART+RDPHASE_2

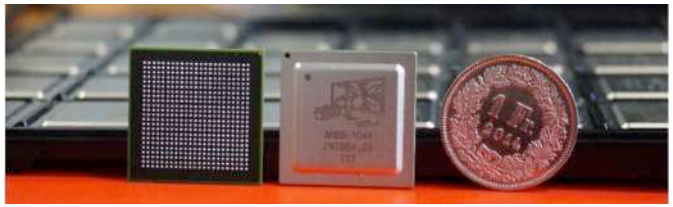
- **AM07 chips will be** designed and characterized within the project for several disciplines:
  - **Image analysis**
  - **DNA sequencing**
  - **Trigger DAQ**

65 nm → 65 nm → 28 nm + FPGA

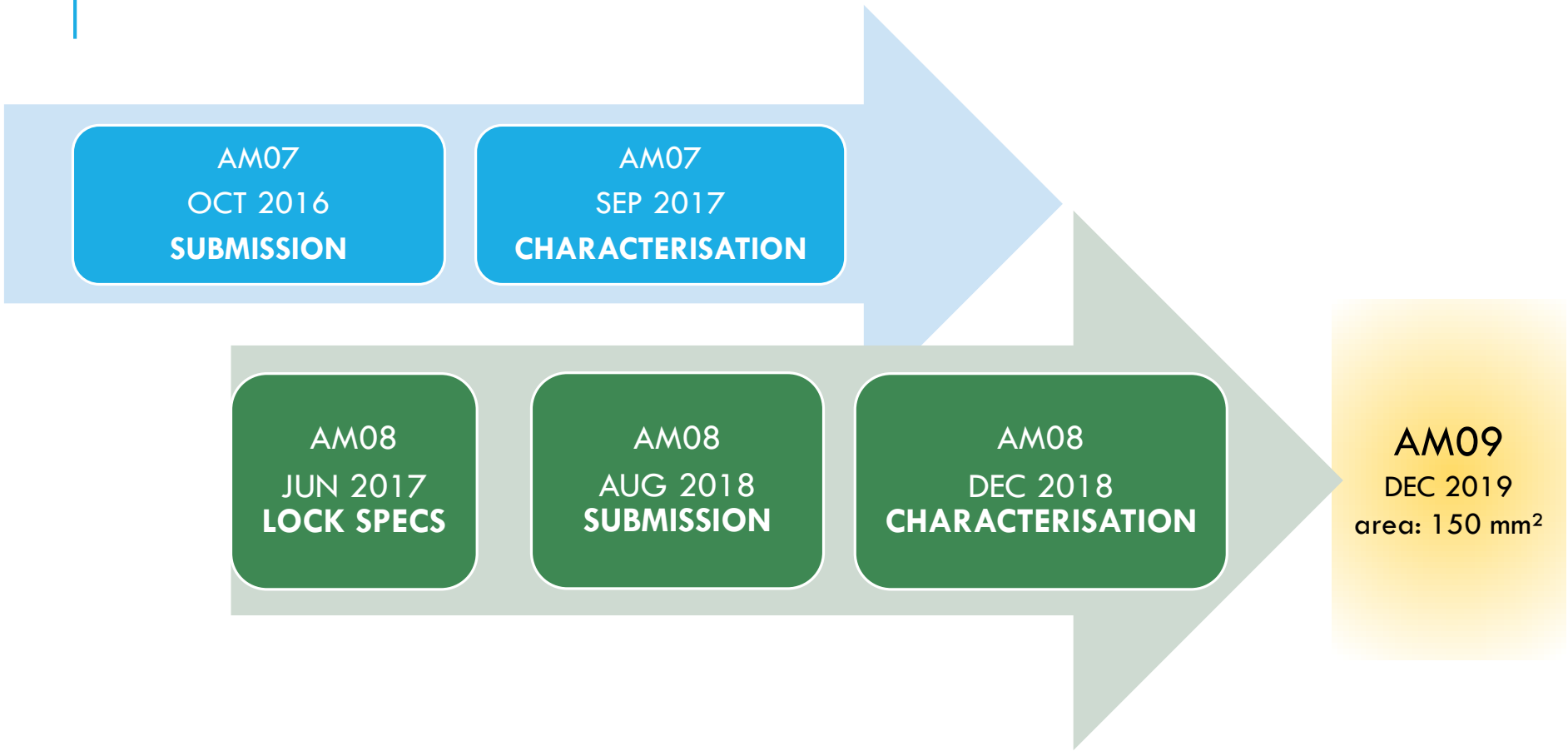
Since 2011:

- **AM chip v. 5-mini@sic** designed and characterized 2012 – area: 4 mm² – cost: 20 k€ – 256 pattens for cell test
- **AM chip v. 5-mpw** designed and characterized 2013 – area: 12 mm² – cost: 75 k€ – 5 kpattens
- **AM chip v. 6** under design; to be submitted in Dec. 2014 – area: 160 mm² – cost: 550 k€ – 128 kpattens -
  421 millions transistors





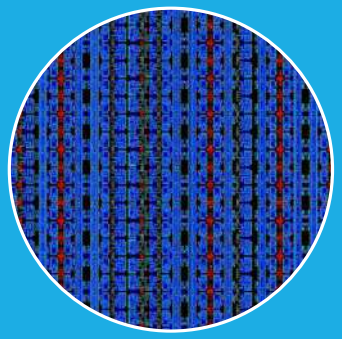
SCHEDULE FOR THE NEXT CHIPS



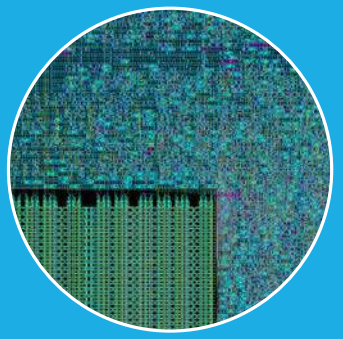
AMCHIP DESIGN COMPLEXITY VS CPUS

Chip name	*Transistor count*	*Year*	*Brand*	*Technology*	*Area*
Core 2 Duo Conroe	291,000,000	2006	Intel	65 nm	143 mm²
Itanium 2 Madison 6M	410,000,000	2003	Intel	130 nm	374 mm²
Core 2 Duo Wolfdale	411,000,000	2007	Intel	45 nm	107 mm²
AM06	**421,000,000**	**2014**	**AMteam**	**65 nm**	**168 mm²**
Itanium 2 with 9 MB cache	592,000,000	2004	Intel	130 nm	432 mm²
Core i7 (Quad)	731,000,000	2008	Intel	45 nm	263 mm²
Quad-core z196[20]	1,400,000,000	2010	IBM	45 nm	512 mm²
Quad-core + GPU Core i7 Ivy Bridge	1,400,000,000	2012	Intel	22 nm	160 mm²
Quad-core + GPU Core i7 Haswell	1,400,000,000	2014	Intel	22 nm	177 mm²
AM09	**1,684,000,000**	**2019**	**AMteam**	**28 nm**	**150 mm²**
Dual-core Itanium 2	1,700,000,000	2006	Intel	90 nm	596 mm²

DESIGN METHODOLOGY

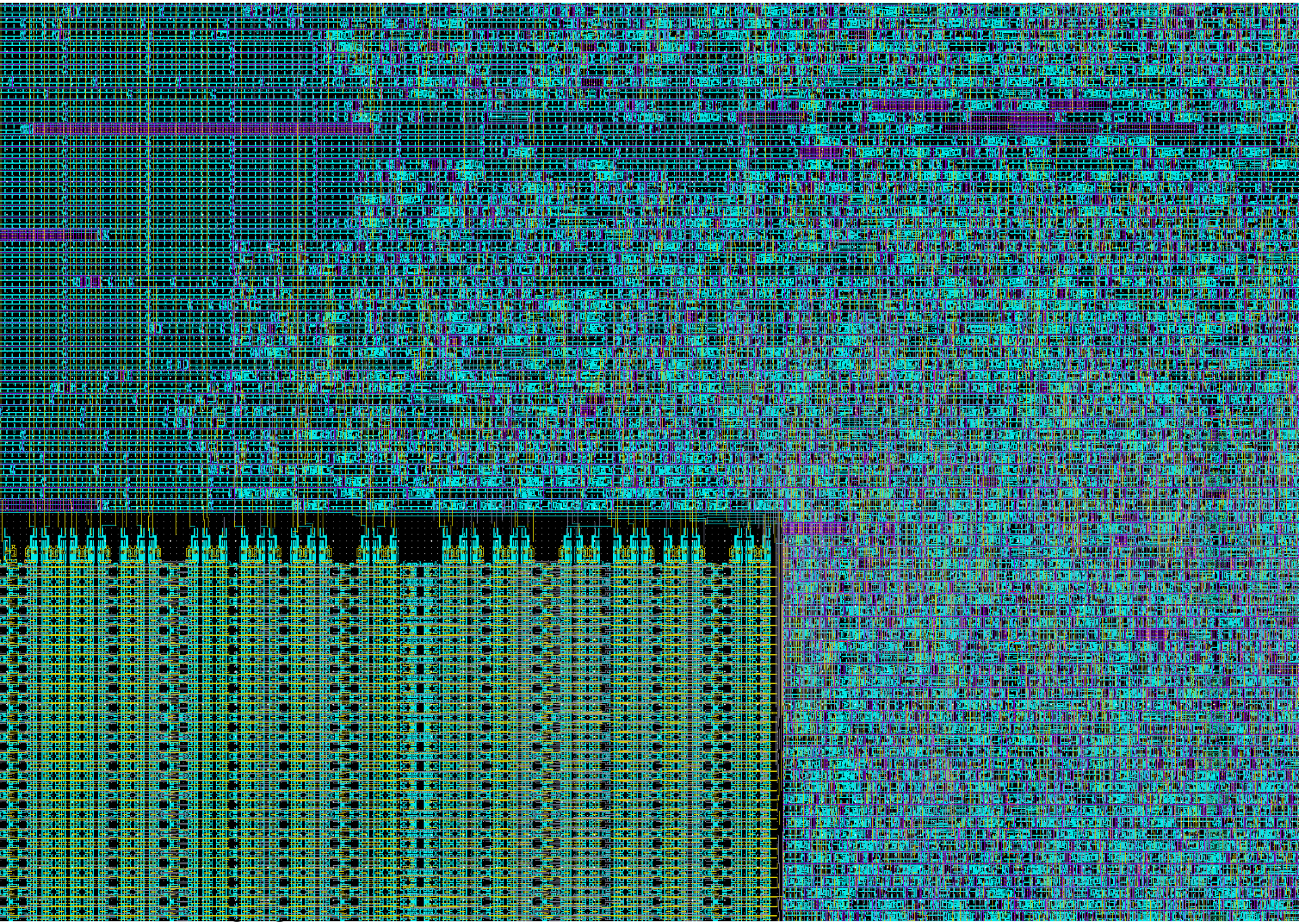


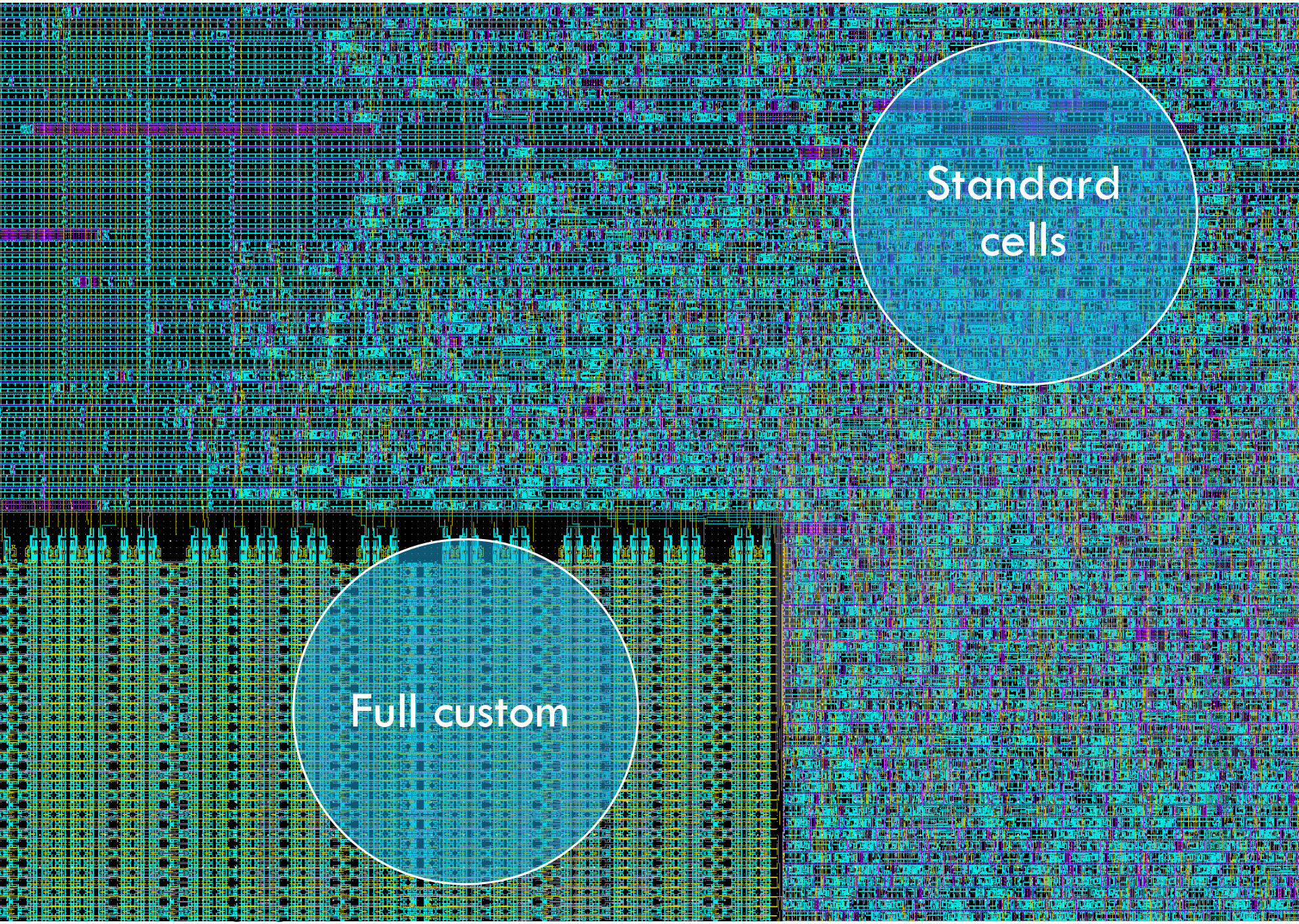
More repetitive parts have been design “by hand” with a full custom approach

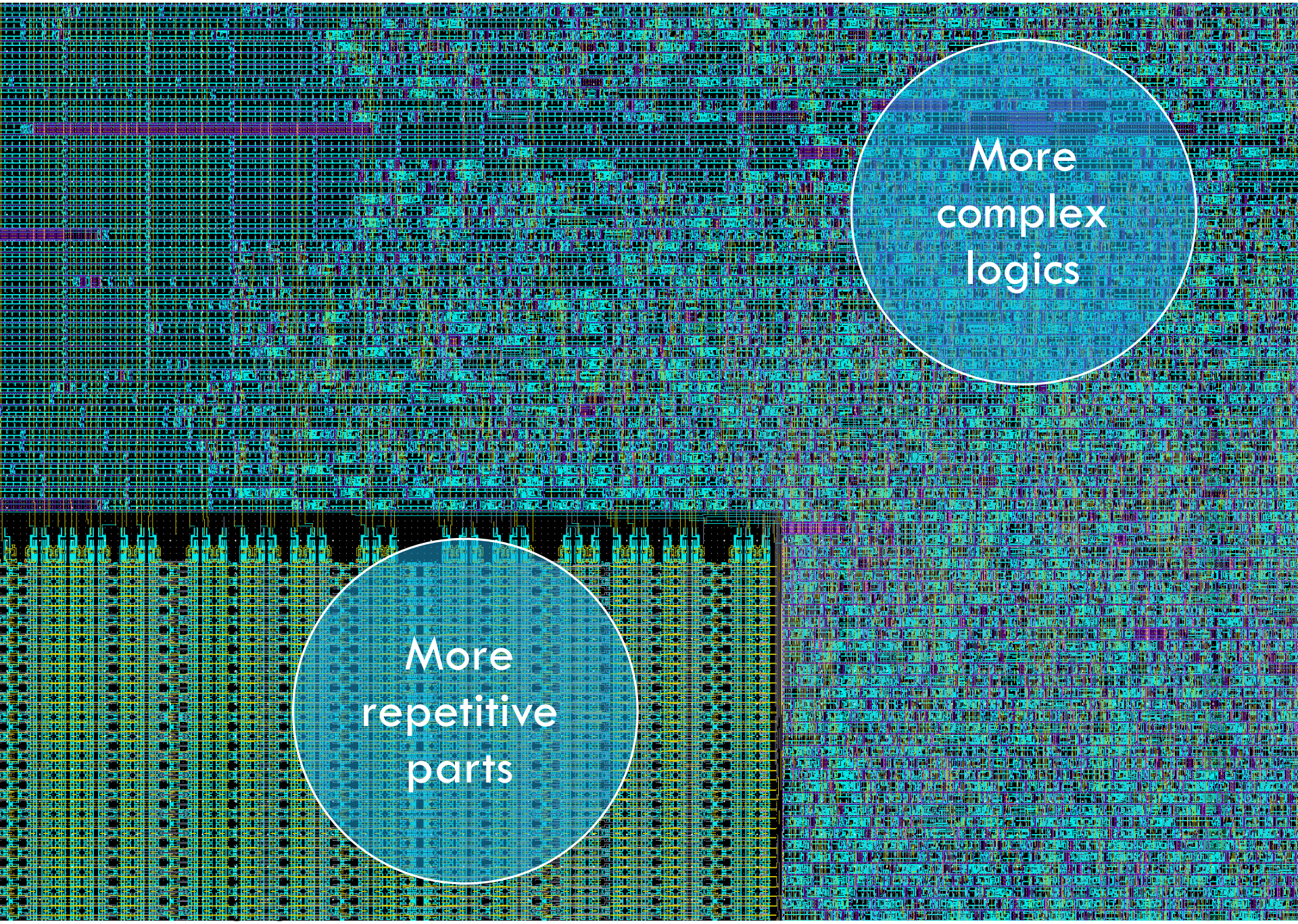


More complex logics have been design with automatic tools based on standard cells (synthesis, place & route)

MIXED APPROACH




Standard cells
Full custom


More complex logics
More repetitive parts

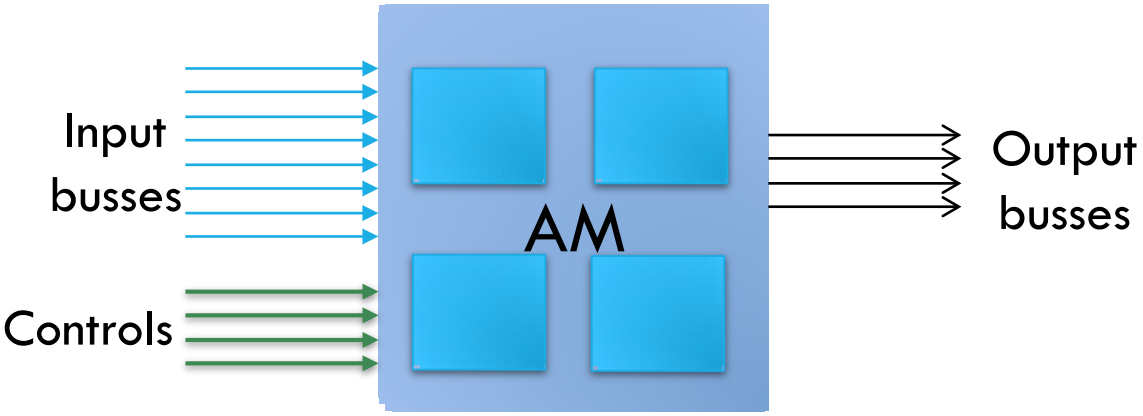
AM09 COMPLEXITY

AM09 will be one of the most complex chips designed within CERN collaboration

Comparison rate:

about 30 peta comparisons per second per chip

MULTI-CORE ARCHITECTURE



Chip will be composed by few **cores**

Outputs could be merged or independed

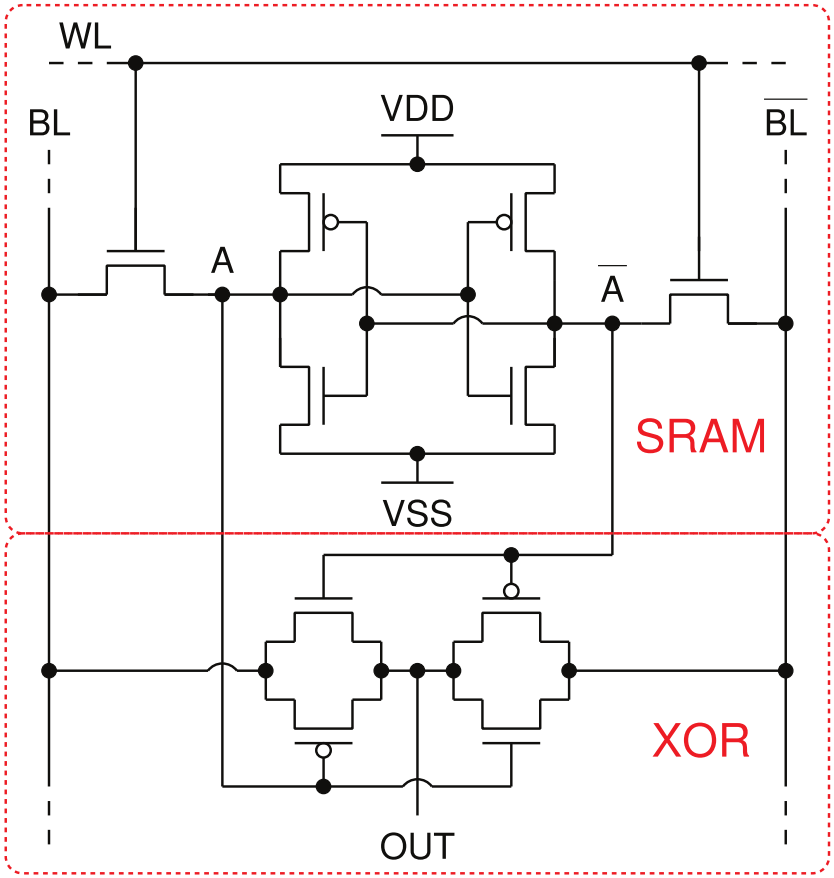
- Choice depending on required output bandwith

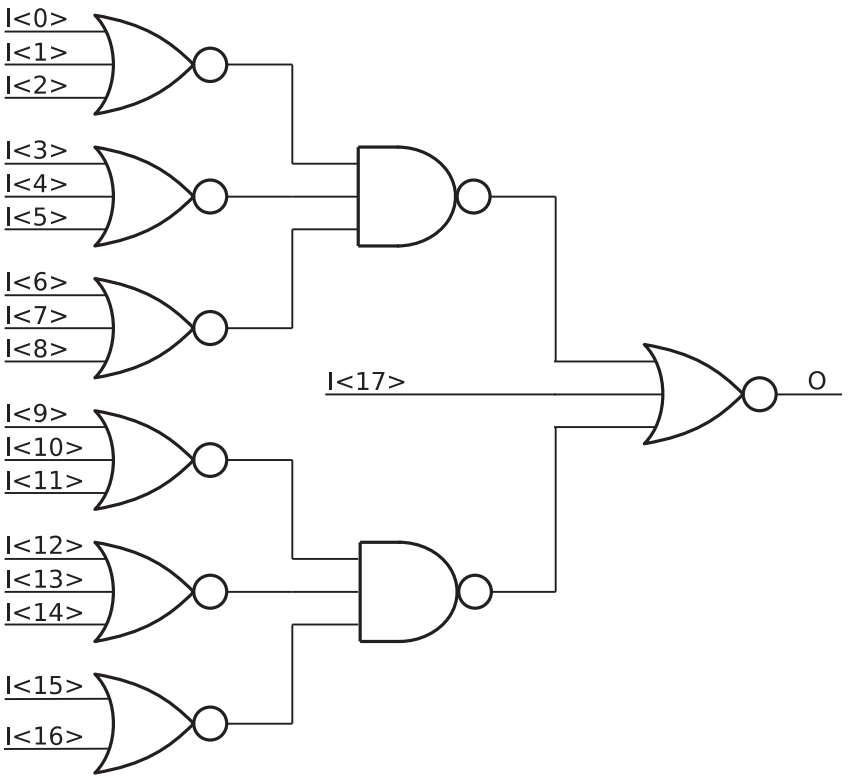
THE XORAM CELL

Based on the previous 65 nm XORAM cell

Based on the XOR boolean function, instead of the NAND and NOR functions

Is made of a 6T SRAM cell connected to a 6T-XOR gate





NEW OPTIMIZED CELLS

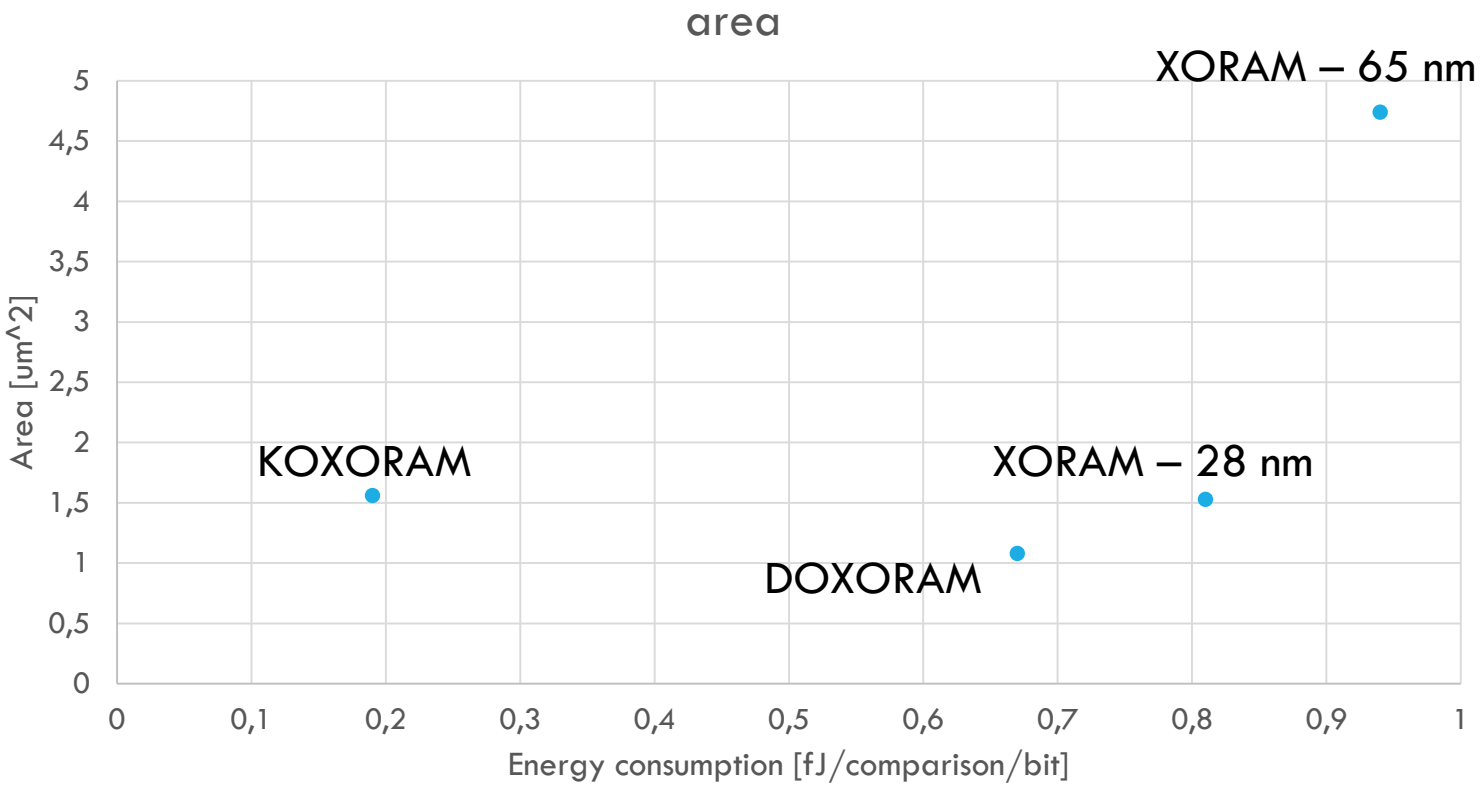
With similar power save methods we designed two new cell tech:

- DOXORAM
- KOXORAM

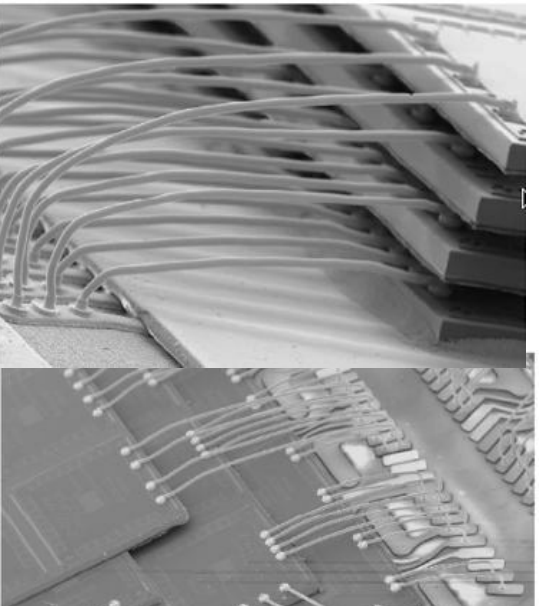
Italian Patent: A. Annovi, L. Frontini, V. Liberali, A. Stabile, "MEMORIA CAM", UA2016A005430

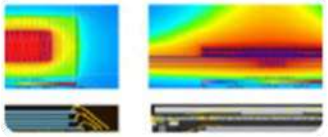
In this week INFN will decide for the internationalization

FULL CUSTOM CELL:
ENERGY CONSUMPTION VS AREA



MULTI PACKAGE





3D assembly technology **studies:**

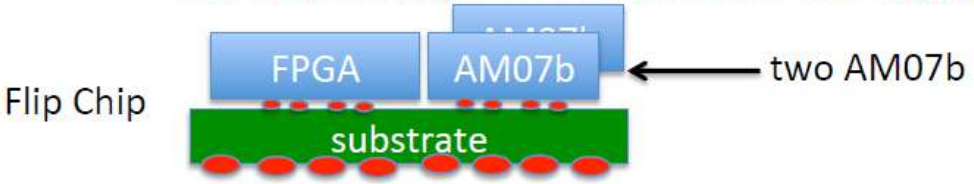
- **Choose technology** which optimize power consumption
- Electrical and thermal **3D simulations** needed
- **Design and test** of the package

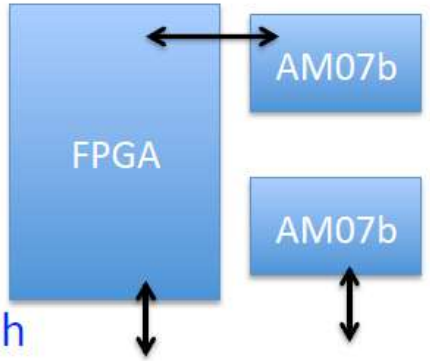
Support by **IMEC** (a micro- and nanoelectronics research center with headquarters in Leuven, Belgium)

- **broad expertise** in multi-chip package technologies

Explore multipackaging

- 1 or 2 AM chip + 1 FPGA in the same package





- Dramatically increases AM to Track Fitter bandwidth
  - "Through Silicon Vias not required!"

28 NM AMCHIP APPLICATIONS

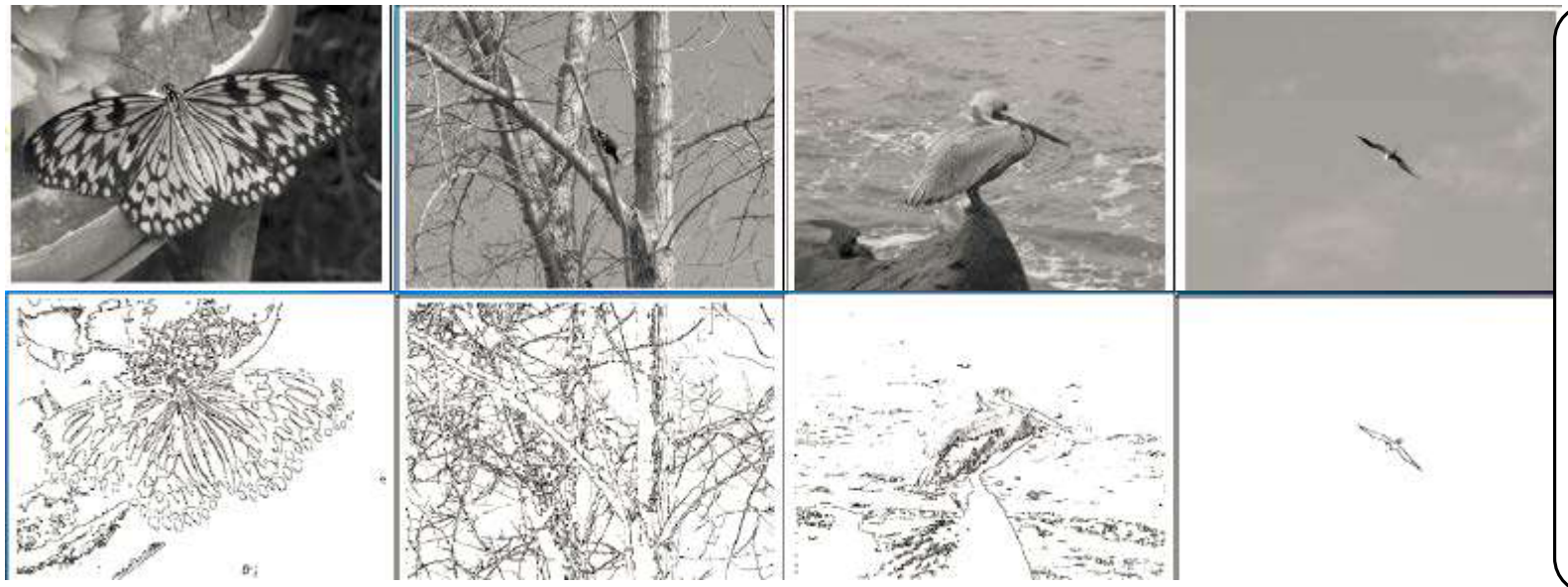
A. Stabile

COMPUTER VISION FOR SMART CAMERAS AND MEDICAL IMAGING APPLICATIONS

Smart cameras capture high-level description of a scene and perform **real-time extraction of meaningful information**

- Current compression algorithms: **few seconds** are required
- **For safety-critical applications (e.g., transports, or personnel tracking in a dangerous environment), latency could lead to serious problems.**

Del Viva et al algorithm[1] studied how to reproduce initial stage of the brain visual processing: find contourns



off-line simulation results

[1] *M. Del Viva, G. Punzi, and D. Benedetti. Information and Perception of Meaningful Patterns. PloS one 8.7 (2013): e69154.*

FUTURE DEVELOPMENTS

Medical application

Automated medical diagnosis:

- Huge amount of image data
  - time-varying images
  - very accurate resolution

Real-time applications for **MRI fingerprint** in collaboration with the INFN-Pisa research group

- Guido Buonincontri's CSN5 funded project in 2015

IMPART-based system **performance:**

- **Human exome:** 1.5 % subset of the human genome (25 million nucleotide pairs)
- **Nucleotide encoding:** FASTA format (at least 4 bits are needed)
- Whole exome alignment with **this device: ~ 4 s**

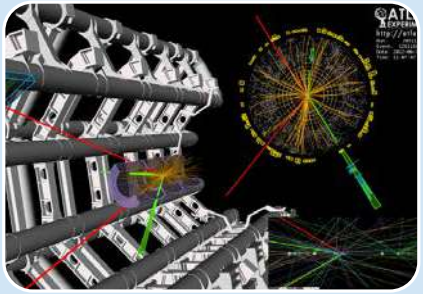
Commercial machines **performance:**

- Bowtie based machines: **1 CPU hour**

Speed improvement factor is about 900x

DNA application

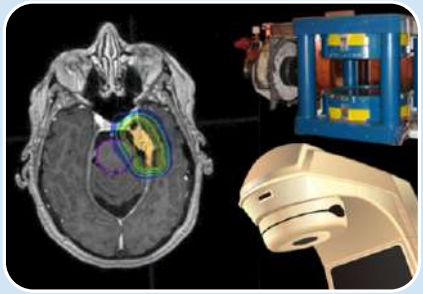
CONCLUSION AND SOCIAL IMPACT



This innovative systems ameliorate the efficiency of many **HEP trigger system**

Smart cameras with this system could be installed in remote environments (forests or mountains)

DNA sequencing could benefit from the project



The system could be also used to **better filtering the fingerprint magnetic resonance images (MRI)**

Several applications could benefit from the project outcome.

THANKS! ☺

Others projects within the microelectronic group:

- Analog amplifiers (A. Pullia, S. Capra)
- 65 nm CMOS readout circuits (V. Liberali, L. Frontini)
- Radiation hard ASICs for aerospace applications (V. Liberali, L. Frontini, A. Stabile)
- Logic syntesis for emerging technologies (V. Liberali, L. Frontini)
- Crosstalk and substrate analysis for automotive (V. Liberali)

BACKUP

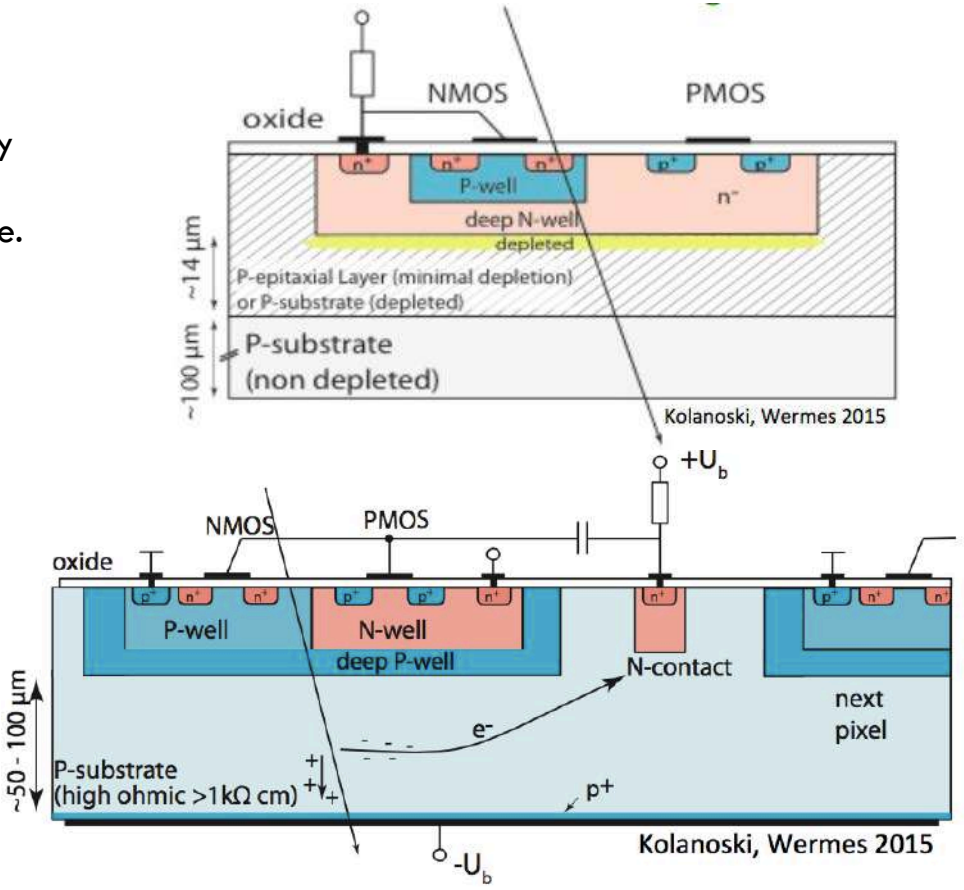
DEPLETION TECHNOLOGIES

OPTION A

- Depletion zone built in a 10-30 µm mid-resistivity p-type epitaxial layer,
- Growth on top of an undepleted p-type substrate.
  - Can be fully depleted with ~ few V
  - Signal 1-2 ke
- Example: AMS, TowerJazz

OPTION B

- Collection electrode is a deep n-well or a buried n-layer,
- Direct implant onto a p-type substrate.
  - Size of depleted region limited by the breakdown voltage
    (technology dependent)
  - Signal up to 10-20 ke (varying with irradiation)
- Example: LFoundry, STMicroelectronics



AMCHIP APPROACH

Two common memory devices are RAMs and CAMs. The Associative Memory is an evolution over the concept of CAM

Type	Function	Application
RAM	write `data` at `address` read `data` from `address`	common memory device used for data storage in information technology
CAM	write `data` at `address` find `addresses` that match `data`	sparse database search, cache, routing tables
AM	write **`segmented data`** at `address` find `addresses` that match a combination of segments within a **`data sample`**	combinatorial pattern matching, CDF SVT, ATLAS FTK, in future CMS, ATLAS FTK++, and interdisciplinary application with IMPART and IAPP

It is more than a memory device, it is an engine to solve a class of combinatorial problem

AM07 ARCHITETURAL FEATURES

- Area: 10 mm²
- Memory depth: 16 kpatterns
- 400 bumps
- 4 independent cores
- LVDS or LVCMOS interface
- Working frequency: 200 MHz

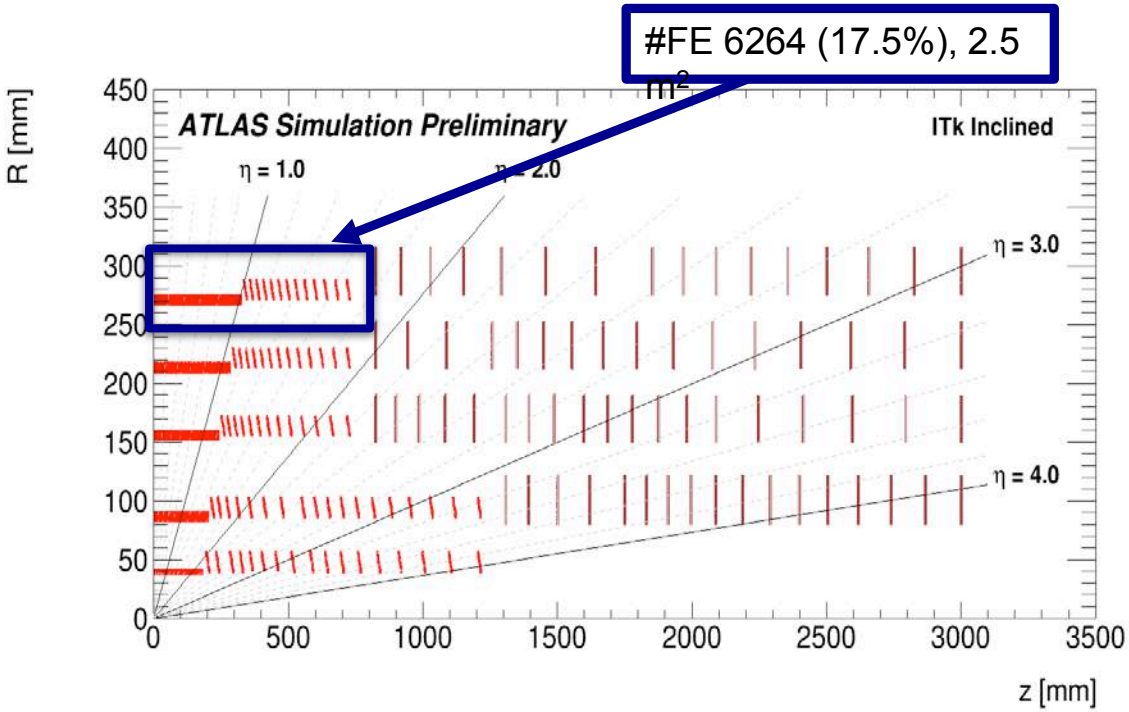
HV-CMOS FOR ATLAS

Monolithic CMOS detector are an interesting option for ATLAS ITk

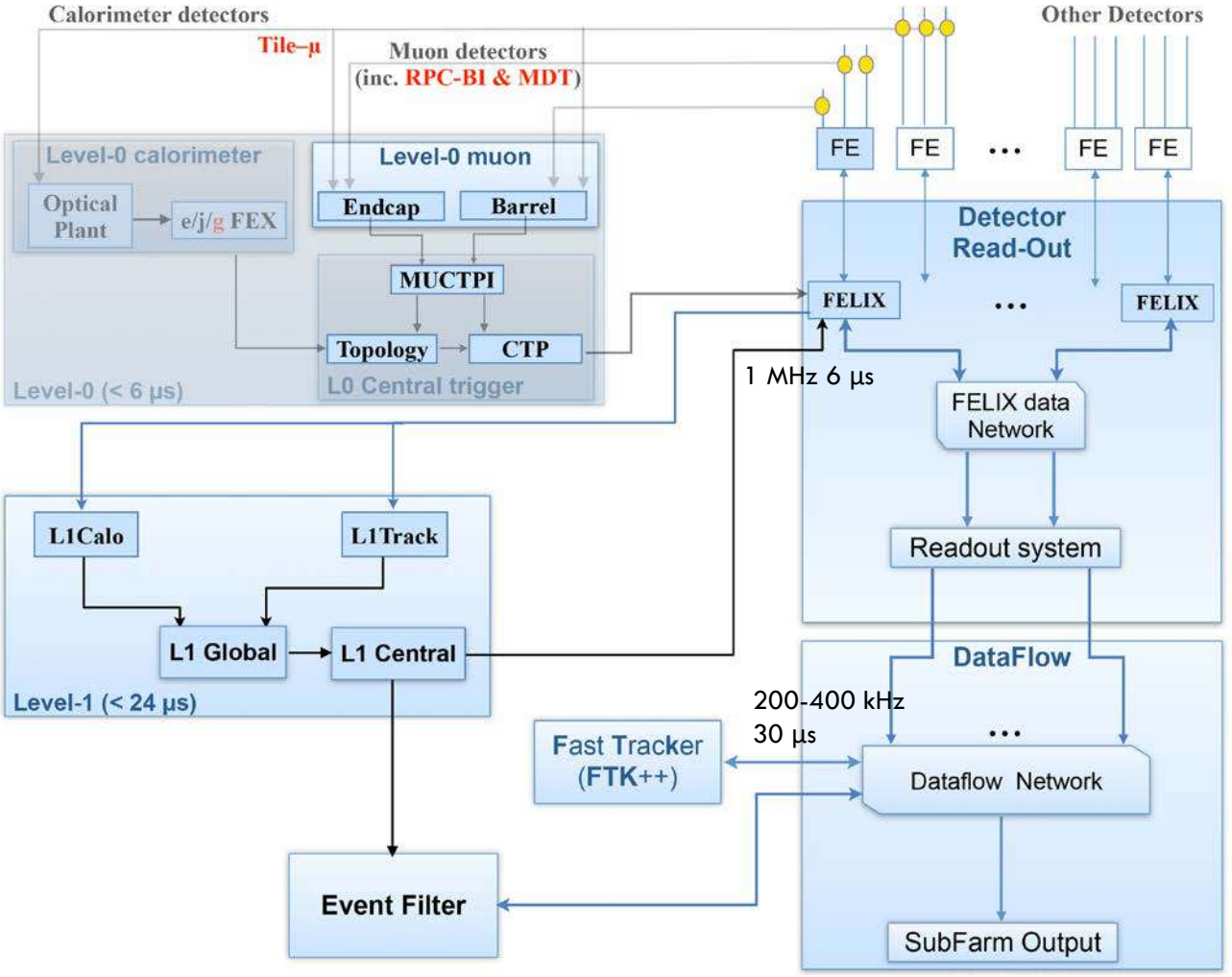
- reduction of material, simplification of assembly, potential reduction of power consumption

Candidate application is for the **outermost pixel layer**

- largest area layer, where practical benefits are outstanding
- reducing pressure on bump bonding and simplifying the assembly, it provides contingency to the whole pixel project
- radiation level and data rates comparable with current IBL/L0:
  NIEL 1.2×10^{15} n_{eq}/cm^2,
  TID 60 Mrad,
  hit rate 0.9 MHz/mm^2
- compatible with the 130-180 nm integration level provided by HV/HR technologies



ATLAS APPROACH

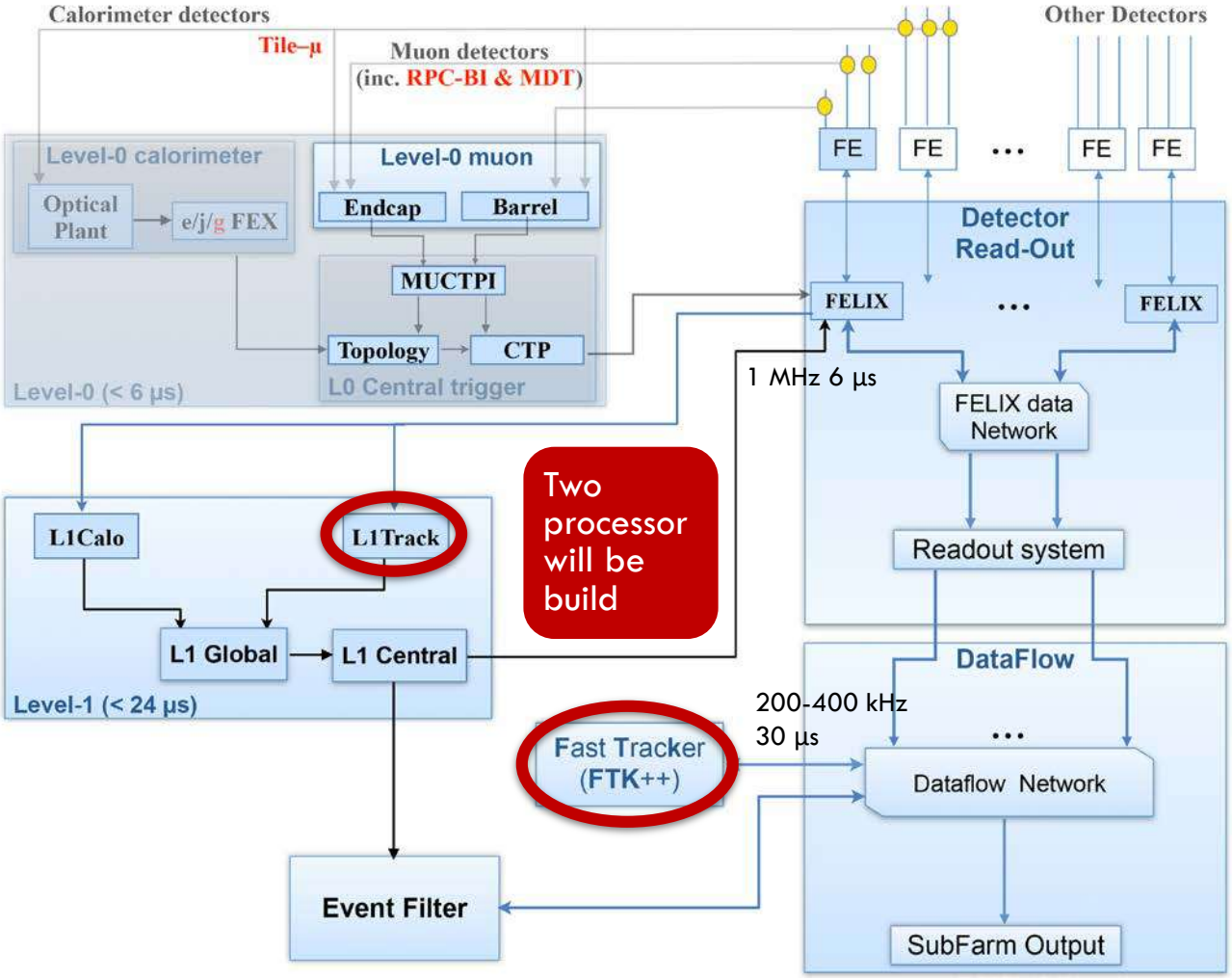


AM06 DESIGN COMPLEXITY

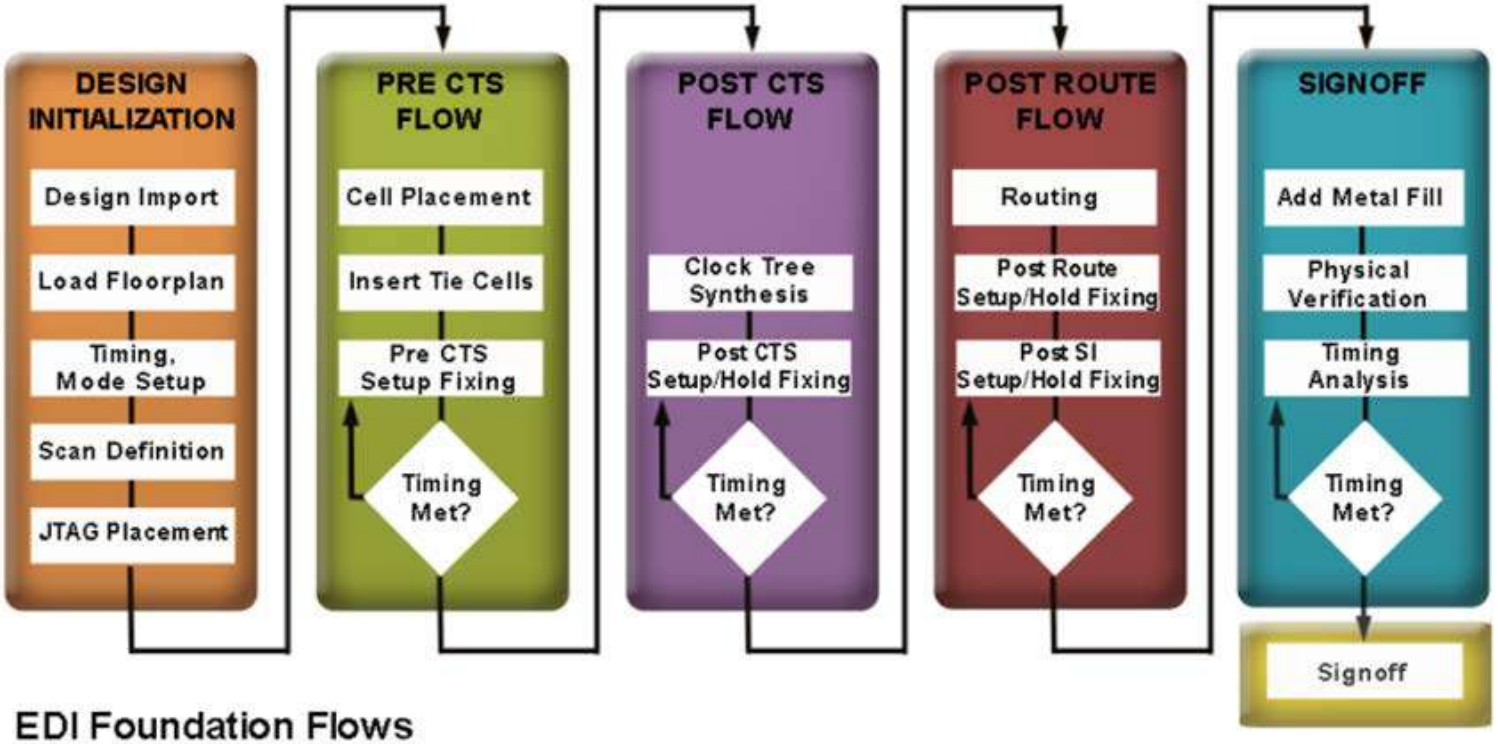
Silicon area	• 14.68 mm x 11.44 mm
Transistors	
Standard cells	• 20.5 millions
Pad	• 964
4096 XORAM block (full-custom design)	• 62740 transistors inside one XORAM block • 22.400 nets inside one XORAM block

New electronics being designed for 6 µs and 30 µs respectively

ATLAS APPROACH



FOUNDATION FLOW (PLACE & ROUTE)



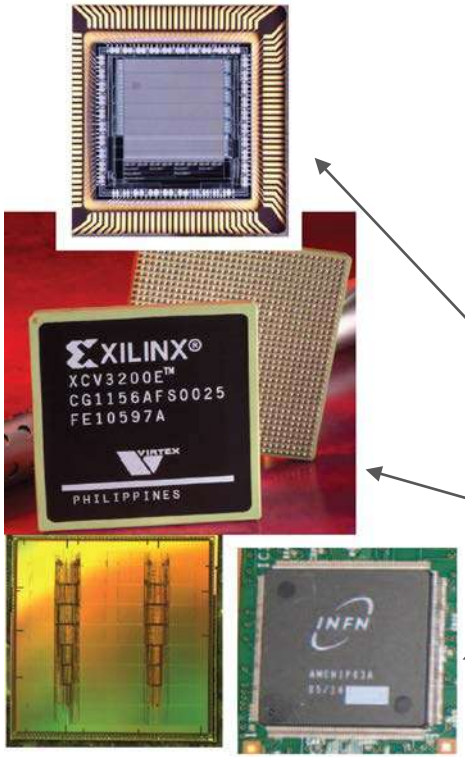
EDI Foundation Flows

cadence

DEDICATED HARDWARE

Pattern recognition problem can be solved by an **Associative Memory (AM) chip**

Integrated circuit	**Content Addressable memory**	Maximum level of **parallelism**	**Comparison** of input data with a set of precomputed patterns stored in a memory	**Select few tracks** among several tracks



1990: AM chip v.1 – ASIC CMOS 700 nm with 128 patterns

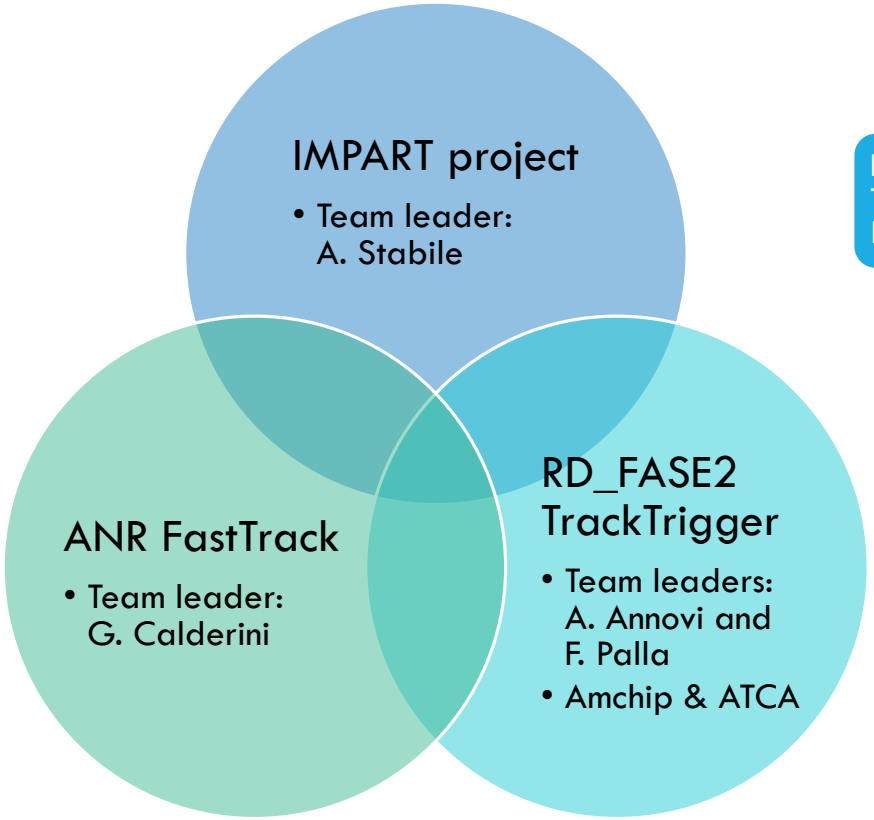
1998: AM chip v.2 – FPGA same of AM chip v.1

2004: AM chip v.3 – ASIC CMOS 180 nm with 5000 patterns

FUNDING AND PEOPLE

Alberto Stabile

FUNDING PROJECTS



Firmware: C. GENTSOS
TIPP2014:The Fast TracKer Processing Unit future evolution

PIXEL PROJECT: HUMAN RESOURCES

Institute	FTE 2017/18	FTE 2018/19	Persons involved	Tasks
Milano INFN and UNIMI	2.5	2.5	Valentino Liberali, Alberto Stabile, Luca Frontini, Stefano Capra	Redesign CAMs, majority, readout, DCO, Integration in Encounter Tempus, Coordination, Package Design, PDN analysis, Signoff, Characterisation AMs
Lyon IPNL	1.5	1.5	Sebastien Viret, Guillaume Baulieu	CMS simulation and demonstrator development.
University of Melbourne	1.2	1.2	Takashi Kubota, Jafar Shojai	VHDL and UVM, AMS, Characterization AMs, Design direct access circuitry for the CAMs
Paris LPNHE	1	1	Francesco Crescioli, Maroua Garci	Redesign CAMs, PLL, VHDL, Integration, Signoff, Characterization AMs
University of Bergamo	1	1	Francesco De Canio, Gianluca Traversi	Reference current, Temperature sensor, I/O optimization.
Pisa INFN and UNIPI	0.5	0.5	Alberto Annovi, Calliope Sotiropoulou, Fabrizio Palla, Giacomo Fedi, Guido Buonincontri	Physics coordination, Image Analysis and MRI (if we found new people)
Total	***7.7***	***7.7***		

AM PROJECT: HUMAN RESOURCES

Institute	FTE 2017/18	FTE 2018/19	Persons involved	Tasks
Milano INFN and UNIMI	2.5	2.5	Valentino Liberali, Alberto Stabile, Luca Frontini, Stefano Capra	Redesign CAMs, majority, readout, DCO, Integration in Encounter Tempus, Coordination, Package Design, PDN analysis, Signoff, Characterisation AMs
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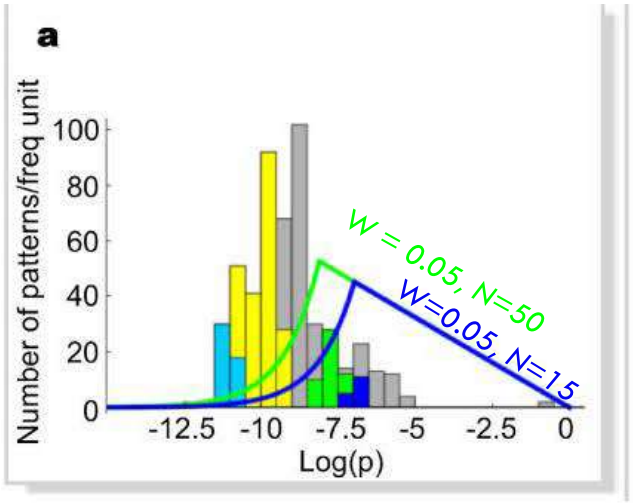
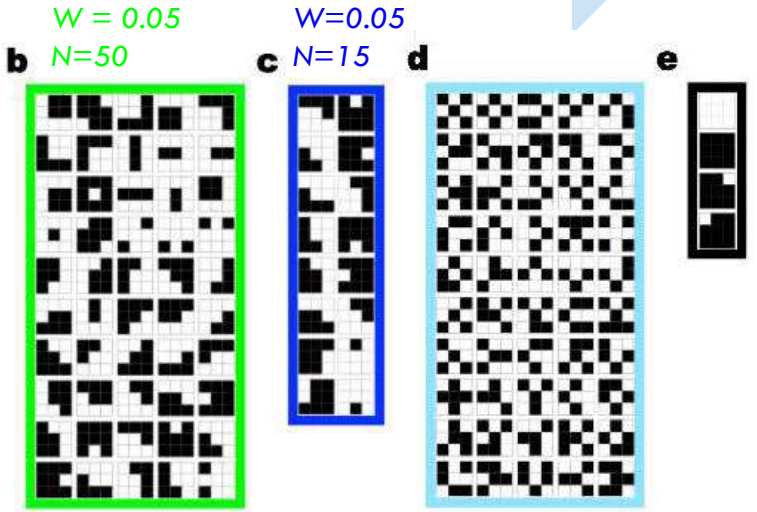
PATTERN SELECTION

Training phase | **Pattern selection** | Writing operation | Real-time pattern recognition | Output formatting operation | Clustering operation | Shape recognition





highest probability patterns (resembling uniform luminance)

lowest-probability Patterns resembling visual noise

Probability distribution of the $N_{tot}=2^9$ possible 3×3 square pixel matrices in black-and-white (1-bit depth) for natural images.

PRELIMINARY RESULTS

four levels of grey